



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,921	11/13/2003	Chang Yeol Lee	CU-3455 RJS	9872
26530	7590	05/17/2005	EXAMINER	
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1200 CHICAGO, IL 60604			CHEN, JACK S J	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/712,921	Applicant(s) LEE ET AL.	
	Examiner Jack Chen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2005.
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
 4a) Of the above claim(s) 5-10 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-4 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2813

DETAILED ACTION

In response to the communication filed on March 8, 2005, claims 1-10 are active in this application.

Applicant's election of Species I (figs. 3a-3d) in the reply filed on March 8, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant indicated that claims 1-4 read on the elected Species I is noted. Accordingly, claims 5-10 are withdrawn from further consideration.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Oath/Declaration

Oath/Declaration filed on November 13, 2003 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Art Unit: 2813

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itonaga et al, U.S./6,800,512 B1 in view of Yamazaki, U.S./6,573,575 B1

Itonaga et al. teaches a method for forming a semiconductor device, which comprises forming an STI oxide film 12 at proper sites of a silicon substrate having an NMOS forming region Rn and a PMOS forming region Rp (fig. 5a); sequentially forming a gate dielectric film 17a/17b and a polysilicon film 18 (fig. 5b) on the silicon substrate including the STI oxide film; selectively implanting an N-type impurity (fig. 5c) and a P-type impurity into (fig. 5b) the portions of the polysilicon film, which correspond respectively to the NMOS forming region and PMOS forming region of the silicon substrate, by ion implantation; and patterning the polysilicon film having the selectively ion-implanted N-type and P-type impurities and the gate dielectric film to form an N+ polysilicon gate 18b (fig. 6d) in the NMOS region of the silicon substrate and a P+ polysilicon gate 18a (fig. 6d) in the PMOS region of the silicon substrate, wherein the ion implantation of the N-type impurity is performed by implanting phosphorus, see figs. 1-26 and cols. 1-28 for more details.

Re claim 2, wherein said STI oxide film is formed higher than the surface of the silicon substrate (fig. 4a).

Re claim 3, wherein said polysilicon film has a thickness ranging from 1900 to 2100 angstroms (i.e., 2000 angstroms, see col. 14, lines 54-56).

Re claim 4, wherein said polysilicon film is formed relatively thicker at fringing portions where it adjoins the STI oxide film and the silicon substrate (fig. 5b).

Itonaga disclosed above; however, Itonaga is silent to implanting phosphorus in a dose of $1 \text{ to } 2 \times 10^{16}/\text{cm}^2$.

Yamazaki teaches a method for forming semiconductor device, which comprises forming NMOS device by implanting phosphorus in a dose of $1 \text{ to } 2 \times 10^{16}/\text{cm}^2$ (i.e., $1 \times 10^{16}/\text{cm}^2$) into the polysilicon layer (fig. 3C) in order to provide low threshold voltage for the NMOS, see figs. 1-6B and cols. 1-10 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to select the suitable implanting dosage as taught by Yamazaki in the method of Itonaga et al. in order to provide low threshold voltage for the NMOS.

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Itonaga et al. by selecting the suitable thickness for the polysilicon layer and suitable implanting dosage for the polysilicon layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

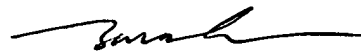
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen
Primary Examiner
Art Unit 2813

May 15, 2005